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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,169	07/14/2003	Francisco Javier Guerrero Mercado	P05514 (NAT115-05514)	5012
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			2816	

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/619,169

Applicant(s)

GUERRERO MERCADO,
FRANCISCO JAVIER

Examiner

Tuan T. Lam

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 July 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-3, 7-11 and 15-20 is/are rejected.
7) ☒ Claim(s) 4-6 and 12-14 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 10 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the amendment filed 7/25/2005. Claims 1-20 are pending and are under examination.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 7-8 and 15-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In this instant, the specification has failed to describe as to how “the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock” of claim 7 is made and/or used. Page 13, lines 12-14 of the specification has briefly mentioned that “pulse generator produces a 390ns wide pulse on every falling edge of the clock signal, and the comparator output is sampled with the clock signal’s rising edge”. Figure 3 shows a block diagram labeled as “Pulse Generator” 301. A careful examination of the block diagram 301, it is noted that there is not clock signal being shown. Similarly, the comparator 100 does not show the clock signal. Therefore, it is unclear as to how the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock is performed without undue experimentation. Clarification and correction are required.

Regarding claims 8 and 17, the specification fails to describe as to how “the comparator selectively operates in a first mode in which the input gain stage is biased by a bias current with a defined first level value or in a second mode in which the input gain stage is biased a bias current with a different second level value” is enabled. Page 11, lines 6-25; page 12, lines 1-25 of the specification uses waveforms diagrams of figures 2A to 2C discusses the slow and fast operational modes of the comparator. Figures 4A and 4B shows the detailed structure of the comparator. **However, it is unclear as to how the circuit shown in figures 4A and 4B enable operatively in first and second modes** as called for in claim 8. That is, it is unclear as to how the comparator is selected to operate in a first mode in which the input gain stage is biased by a bias current with a defined first level value or when the comparator is selected to operate in a second mode the input gain stage is biased a bias current with a different second level value without undue experimentation. Applicant is required to particularly point out the recited features.

Claims 15 and 16 are rejected for the same reasons as claims 7 and 8, respectively.

Regarding claim 19, the specification fails to describe as to how the “current source biased by the pulsed or continuous bias current and controlled by the input signal” is enabled. Figure 1 shows “**an equivalent circuit**” of the actual present invention. The equivalent circuit shows a symbol of a variable current (i_{bias}) being received a symbolic gm signal. Page 11, lines 6-25; page 12, lines 1-25 of the specification uses waveforms diagrams of figures 2A to 2C discusses the slow and fast operational modes of the comparator. Figures 4A and 4B shows the detailed structure of the comparator. **However, it is unclear as to how the current source being biased by the pulse or continuous bias current and controlled by the input current**

Art Unit: 2816

would correspond to the actual components of the actual comparator shown in figures 4A and 4B. Therefore, it is unclear as to how current source biased by the pulsed or continuous bias current and controlled the input signal” is achieved without undue experimentation.

Claims 18 and 20 are rejected under 35USC 112, first paragraph because of the technical deficiencies of claim 17.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Lim (USP 5,841,306). Figure 4 of Lim shows an integrated circuit comparator comprising an input receiving an input signal (current along collector/emitter of transistors Q8, Q9) representative of a difference between quantities to be compared (V_{th} , V_{ref}), an input gain stage (Q8, Q9, R7, R8) receiving the input signal and biased with a pulsed bias current (current (b) at the collector of transistor Q7, the waveform of the current is shown in figure 5C. The current (b) is pulse current), the input gain stage producing a gain based upon the input signal as called for in claims 1, 9.

Regarding claims 2 and 10, the input signal is a current representative of transconductance of a differential pair of input transistors (Q8, Q9).

Regarding claims 3 and 11, the input gain stage further comprises a current source (Q5, Q7) biased by the pulsed bias current (the current version of the V_{tri} at the collector of transistor

Art Unit: 2816

Q2) and controlled by the input signal (/Tout is the inverted version of Tout where Tout is output version of the input signal, e.g., signal along collector and emitter of Q8).

3. Claims 1-3, 8-11 and 16, 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Heinrich (USP 6,323,695).

Figure 1 of Heinrich shows an integrated circuit comparator comprising an input receiving an input signal representative of a difference between quantities to be compared (U and Vref), an input gain stage (T1, T2, T3, Sp4) receiving the input signal and biased with a pulsed bias current (Ic current signal at node S, the waveform of the current is shown in figure 3. The current is a pulse current), the input gain stage producing a gain based upon the input signal as called for in claims 1, 9 and 17.

Regarding claims 2 and 10, the input signal is a current representative of transconductance of a differential pair of input transistors (T1, T2).

Regarding claims 3 and 11, the input gain stage further comprises a current source (Sp4) biased by the pulsed bias current (Ic at node S) and controlled by the input signal (U).

Regarding claims 8 and 16, wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a bias current with a defined first level (figures 2 and 3, the constant current Ic1 at t0, t2 and t4 periods) or in a second mode in which the input gain stage is biased a bias current with a different second level value (pulsed current Ic1 at t1 and t3).

Regarding claim 17, figure 1 of Heinrich shows a comparator selectively operating in a first mode in which an input gain stage (T1, T, Sp5, Sp4) of the comparator is biased with a pulsed bias current (Ic1 is pulse in the periods t1, t3) and a second mode in which the input gain

stage is biased with a continuous bias current (constant current at periods t0, t2 and t4 are supplied to the input gain stage in a second mode of operation).

Regarding claim 18, the input gain stage receives an input (U-Vref) representing the different between U and Vref and produces a gain based upon a current for the input signal representative of transconductance of a differential pair of input transistors (T1, T2).

Regarding claim 19, figure 1 shows the input gain stage further comprises a current source (Sp4) biased by the pulsed bias current (Ic at node S) and controlled by the input signal (U).

Response to Arguments

4. Applicant's arguments filed 7/25/2005 have been fully considered but they are not persuasive.

35USC 112, first paragraph:

Regarding the rejection of claims 7 and 15 under 35USC 112, first paragraph as the specification has failed to describe in such a way to enable one skilled in the art to make and/or use of the present invention, applicant argues that the test of enablement is whether one skilled in the art could make and use of the invention from the disclosures without undue experimentation.

Applicant further stated that it was well-known in the art at the time the instant application was ~~filed~~^{filed} that a global or "system" clock be used to coordinately control various components or logical units within an integrated circuit. Such signals are understood to exist and generally are NOT depicted in high level drawings (e.g., functional unit drawings, as opposed to circuit diagrams). Thus, those skilled in the art would not be confused by the absence of an expressly depicted system clock signal within a functional drawing of an integrated circuit. Applicant is

Art Unit: 2816

right about global or system clock signal. However, it is still unclear as to how the pulsed biased current is generated from the system clock. This pulsed biased current is being used to bias the input gain stage, one of the inventive features of the present invention, thus providing a gain. The specification briefly mentions the pulse current is produced (page 13, lines 12-14). Since the pulsed current bias is an critical features of the present invention, given from what being disclosed in the specification as mentioned above, it is an undue experimentation for one skilled in the art to produce a pulse generator that are capable of generating the pulsed current bias. Therefore, the rejection is deemed proper.

Regarding the rejection of claims 8 and 17, applicant points out section of page 11, in particular, paragraph 0023 to support the recited limitations of claims 8 and 17. Paragraph states there are two modes of operation, i.e., low speed mode and high speed mode. Each mode of operation is driven with different bias current values. However, the specification has failed to describe as to how the mode of operation is selected. Therefore, it is undue experimentation for one skilled in the art to make the comparator whose bias current is at different level as different mode of operation. Therefore, the rejection is deemed proper.

Claims 15 and 16 remains rejected for the same reasons as claims 7 and 8, respectively.

Regarding the rejection of claim 19 as being non-enablement, applicant points to figures 4A and 4B to identify the circuit structure corresponding to the equivalent circuit in figure 1. Applicant stated that the “pos” and “neg” inputs corresponding to the different input pair. However, the applicant was silent at the current source producing the pulsed or continuous bias current and controlled by the input signal. Therefore, it is unclear as to how current source

biased by the pulsed or continuous bias current and controlled the input signal” is achieved without undue experimentation.

Therefore, the rejection of claims 7-8 and 15-20 under 35USC 112, first paragraph is deemed proper.

35USC 102(b):

Regarding claims 1-3 and 10-11 as being anticipated by Lim (USP 5,841,306), applicant argues that Lim does not show input gain stage biased with a pulsed bias current as called for in claims 1-3 and 10-11 is not persuasive. Figure 5C of Lim clearly show the bias current Ib as a pulse current biasing the input gain stage in figure 4. Therefore, the rejection is deemed proper. Claims 1-3 and 10-11 remain rejected as being anticipated by Lim.

Regarding the rejection claims 1-3, 8-11 and 16-17 as being anticipated by Heinrich (USP 6,323,695), applicant argues that Heinrich does not show pulsed bias current as called for in claims 1-3, 8-11 and 16-17 is not persuasive. The current Ic1 in figure 3 having a pulse shape waveform anticipating the limitations called for in claims 1-3, 8-11 and 16-17. Therefore, the rejection is deemed proper.

Allowable Subject Matter

5. Claims 4-6 and 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art has been carefully considered.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2816

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Tuan T. Lam', with a long horizontal flourish extending to the right.

Tuan T. Lam
Primary Examiner
Art Unit 2816

9/10/2005